



## INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Application Number

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**Filing Date**

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***First Named Inventor***

Johannes K. Northoff

**Art Unit**

2811

**Examiner Name**

**Attorney Docket Number**

TRWP123US

Examiner  
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LIN WU, et al.; A Low Jitter 1.25GHz CMOS Analog PLL for Clock Recovery; 0-7803-4455-3/98; IEEE, 1998.

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**G. VAN DER PLAS, et al.**, Systematic Design of a 14-bit 150-MS/s CMOS Current-Steering D/A Converter; Department of Electrical Engineering, Katholieke Universiteit Leuven, ESAT-MICAS; Heverlee, Belgium

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